NAME OFTHE FACULTY : Harish Kumar Kaushik

DISCIPLINE : Computer Engineering

SEMESTER : 3rd

SUBJECT : DIGITAL ELECTRONICS

LESSON PLAN DURATION : 15 weeks (04 Aug 2025 – 26 Nov 2025)

COURSE OUTCOMES

After undergoing this subject, the students will be able to:

CO1: Understand various types of number systems and digital codes.

CO2: Describe the logic gates and able to perform logics simplification.

CO3: Design various combinational circuits

CO4: Develop various sequential circuits.

CO5: Analyze A/D & D/A converters and various memories.

Week	Period	Topic
1	1	**UNIT I** **Number Systems and Codes** 1.1 Introduction to analog and digital signal
	2	1.2 Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa.
	3	1.3 Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction.
2	1	1.4 Concept of code, weighted and non-weighted codes, examples of 8421, BCD, excess- 3 and Gray code.
	2	1.5 Concept of parity, single and double parity and error detection.
	3	Revision
3	1	**UNIT II** **Logic Gates and Logic Simplifications** 2.1 Concept of negative and positive logic
	2	2.2 Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates, NAND and NOR as universal gates.
	3	2.3 Introduction to TTL and CMOS logic families
4	1	2.4 Postulates of Boolean algebra, De Morgan's Theorems. Implementation of Boolean
	2	2.5 Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits
	3	Revision
5	1	Revision
	2	**UNIT III** **Combinational Circuits** 3.1 Half adder, Full adder circuit, design and implementation.
	3	3.2 4 bit adder circuit
6	1	3.3 Four bit decoder circuits for 7 segment display and decoder/driver ICs.
	2	3.4 Basic functions and block diagram of MUX and DEMUX with different ICs
	3	3.5 Basic functions and block diagram of Encoder

7	1	Revision
	2	Revision
	3	**UNIT IV** **Sequential Circuits** 4.1 Concept and types of latch with their working and applications
8	1	4.2 Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops. Difference between a latch and a flip flop
	2	4.2 Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops. Difference between a latch and a flip flop
	3	4.3 Introduction to Asynchronous and Synchronous counters. Binary counters, Divide by N ripple counters, Decade counter, Ring counter
9	1	4.3 Introduction to Asynchronous and Synchronous counters. Binary counters, Divide by N ripple counters, Decade counter, Ring counter
	2	4.4 Introduction and basic concepts including shift left and shift right.
	3	4.4 Introduction and basic concepts including shift left and shift right.
10	1	4.5 Serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out.
	2	4.6 Universal shift register
	3	Revision
11	1	Revision
	2	**UNIT V** **Converters and Memories** 5.1 Working principle of A/D and D/A converters
	3	5.2 Brief idea about different techniques of A/D conversion and study of : a) Stair step Ramp A/D converter
12	1	b) Dual Slope A/D converter c) Successive Approximation A/D Converter
	2	b) Dual Slope A/D converter c) Successive Approximation A/D Converter
	3	5.3 Detail study of : a) Binary Weighted D/A converter
13	1	5.3 Detail study of : a) Binary Weighted D/A converter
	2	b) R/2R ladder D/A converter
	3	b) R/2R ladder D/A converter
14	1	5.4 Applications of A/D and D/A converter.
	2	5.5 Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM),
	3	static and dynamic RAM, introduction to 74181 ALU IC
15	1	Revision
	2	Revision
	3	Revision